A Parallel Device Simulator based on Finite Element Method

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Abstract-As semiconductor industry advances toward nanoscale technology, it comes across many issues (such as short channel, narrow width, hot-electron effects etc.), which need to be addressed in time to continue advancements with Moore's Law. Technology Computer Aided Design provides a huge scope to build an environment which can be used to design and develop future devices, and study their alterations with much ease. In this paper, a parallel 2D/3D framework is presented to simulate semiconductor devices using finite element method. This method is used to discretize essential device equations and later these equations are analyzed by using a suitable methodology to find solution. OpenMP directives are used to parallelize the solution of device equations on many-core processors. To showcase the effectiveness of the method, a pn junction diode and a MOS capacitor are simulated, and the results are validated with TCAD device simulator Sentaurus.

Keywords-Semiconductor devices; Electron Transport; Partial differential equation; Finite element method; Numerical Simulation;

I. INTRODUCTION

Whenever we name the greatest innovations of twentieth century, we undoubtedly call upon the electronics technology, which is backed-up by the advancements in semiconductor devices. TCAD plays an important role in further optimising the current technology and to come up with future devices of different geometries and materials. TCAD helps us approximately predict the behaviour of semiconductor devices by implementing various device physics models such as Drift-Diffusion, Hydrodynamics, Boltzmann (Monte Carlo), Quantum Corrected Boltzmann, Nonequilibrium Greens Function) [1]. These models comprise of a set of equations used to calculate potential and chargecarrier density. Drift-diffusion is one of the widely used fundamental models to simulate sub-micron devices. Here a framework has been developed taking into consideration the drift-diffusion model to simulate sub-micron devices. To simulate any of the models, a large number of partial differential equations (PDEs) need to be solved with appropriate boundary conditions. In case of simple and well-defined geometrical problem, an analytical solution of any model can be ensured, whereas it is a tedious task to find a solution for complex problems. For such problems, the solution of the PDEs can only be found using numerical methods. Anand Bulusu

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The computational complexity of these PDEs increases with the increase in multi-dimensionality and complex quantum mechanics. To numerically find solution of any non-linear PDE, first it needs to be discretized into linear-form for a defined geometry. A variety of discretization methods are used to get numerical solution of these equations such as Finite difference method (FDM), Finite Element Method (FEM), Finite Volume Method (FVM) etc. [2] Most of the popular Electronic Design Automation (EDA) tools, such as Sentaurus [3], Cogenda Genius [4], Atlas [5], Comsol etc. employ FDM as discretization methodology.

Although FDM has an advantage of less computational cost in solving 1D simple geometrical problems, the performance degrades with the increase in complexity and dimension. On the other hand, FEM provides accurate results even with a coarse mesh [6] and can handle complex geometries with variable material characteristics suitably [7]. With scaling of technology, it is quite evident that future devices will be having more complex geometries than traditional devices such as MOSFETs or Dual-gate MOSFETs. Considering the advantages of FEM, in this paper a framework of a parallel device simulator capable of handling 2D/3D geometries, using some open source libraries, such as Fenics [8] and Gmsh [9] is presented. Fenics library makes use of FEM discretization approach to get the solution for weak/variational form of PDEs. Gmsh library is used to generate triangular/tetrahedral mesh for 2D/3D geometries of a device. To achieve faster and accurate results, it is imperative to take advantage of current manycore computing architecture. Here OpenMP [10] directives are used to parallelize the solution of device equations on many-core processors. Parallelization in the framework has been achieved during the assembly process of FEM by using OpenMP directives.

The rest of the paper is organized as follows: In Section II, fundamental device equations for Drift-Diffusion model and other basic equation for charge carrier concentration are discussed. Section III describes implementation details of FEM. Simulation results obtained for different geometric devices are discussed in Section IV. Section V concludes the paper.



II. FORMULATION OF BASIC DEVICE EQUATIONS

To build a framework for a device simulator, a certain procedure is followed for the simulation process [11] by incorporating several device models, as shown in Figure 1. At first, data related to material parameters, device geometry, doping profile and necessary boundary conditions are procured. The whole domain (device geometry) is further divided into smaller domains in order to solve PDEs locally to complete the process of discretization. This step generates a mesh throughout the whole geometry to get the solution over all nodes. Then charge is calculated globally using an initial guess of the solution. Later the Poisson's and continuity equations are solved iteratively in a coupled manner. These coupled equations are solved iteratively until the solution converges to a pre-defined threshold. The implementation of both Poisson's and continuity equations includes Gummel's and Newton-Raphson algorithms [11]. At the end of simulation process, the device current is calculated for specified input parameters.



Figure 1. Process flow of a typical device simulation

Poisson's and electron-hole current continuity equations basically describe the modelling of a number of semiconductor device models [11]. Poisson's equation computes the potential throughout the semiconductor device from a given space-charge profile, whereas the current-continuity equations compute the electron and hole carrier concentration taking into account the potential profile and the total generation-recombination of charge carriers. These fundamental drift-diffusion equations can easily be derived from classical Boltzmann transport equation (BTE) by reviewing moments of BTE [12]. The basic set of these five fundamental device equations (*Poisson's equation, current equations and continuity equations*) are given below.

1) **Poisson's equation**

$$\nabla \cdot (-\epsilon \nabla \phi) = \rho \tag{1}$$

where
$$\rho = q[p - n + N_d - N_a]$$

2) Current equations

$$J_n = qn\mu_n \bigtriangledown \phi + qD_n \bigtriangledown n \tag{2}$$

$$J_p = qp\mu_p \bigtriangledown \phi - qD_p \bigtriangledown p \tag{3}$$

3) Continuity equations

$$\frac{\partial n}{\partial t} = \frac{1}{q} \bigtriangledown \cdot J_n + R_n \tag{4}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \bigtriangledown \cdot J_p + R_p \tag{5}$$

where ϕ is potential, μ is mobility, ρ is space charge density, D is diffusion coefficient, R is the net generation and recombination rate, n & p specifies the electron and hole density in the conduction and valance band respectively, q is the electron charge, J is current density, ϵ is dielectric permittivity and t denotes the time.

In order to solve these self-consistent equations we need to formulate equations for n and p in terms of other dependent variables such as, V, ϕ_n and ϕ_p (where ϕ_n , ϕ_p are the quasi-Fermi potentials of electrons and holes respectively). Considering the case of a simple pn junction, the relationship of carrier concentration with the quasi-Fermi potential [13] is as represented in following equations.

The concentration of electron at equilibrium, n_0 in the conduction band (n-region) is given by,

$$n_0 = N_c \exp\left[\frac{-(E_c - E_F)}{kT}\right] \tag{6}$$

where N_c is effective density of states, E_c and E_F are the energy of conduction and Fermi level respectively.

This equation can also be written in the form of intrinsic carrier concentration, n_i and intrinsic Fermi energy, E_{Fi} as:

$$n_0 = N_d = n_i \exp\left[\frac{E_F - E_{Fi}}{kT}\right] \tag{7}$$

and potential ϕ_{Fn} in the n-region is defined as:

$$q \phi_{Fn} = E_{Fi} - E_F \tag{8}$$

Similarly in the p-region, the hole concentration is given by,

$$p_0 = N_v \exp\left[\frac{-(E_F - E_v)}{kT}\right] \tag{9}$$

$$p_0 = N_a = n_i \exp\left[\frac{E_{Fi} - E_F}{kT}\right]$$
(10)

$$q\phi_{Fp} = E_{Fi} - E_F \tag{11}$$

The built-in potential barrier, V_{bi} of a pn junction can be written in the form of quasi-Fermi levels as,

$$V_{bi} = |\phi_{Fn}| + |\phi_{Fp}| \tag{12}$$

Using above mentioned equations for carrier concentration and rearranging them gives the built-in potential as,

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_a N_d}{n_i^2}\right) \tag{13}$$

$$= V_t \ln\left(\frac{N_a N_d}{n_i^2}\right) \tag{14}$$

where E_c , E_v , E_F are the energy levels corresponding to the conduction band, valence band and Fermi level respectively. E_{Fn} and E_{Fp} are the quasi-Fermi energy levels corresponding to electrons and holes respectively, N_a and N_d are the acceptor and donor doping concentrations, N_c and N_v denote the effective density of states for conduction band and valence band respectively and V_t (= kT/q) represents thermal voltage.

The Space-Charge width, x_p of a pn junction can be described as,

$$x_p = \frac{N_d \times x_n}{N_a} \tag{15}$$

$$x_n = \left\{ \frac{2\epsilon_s V_{bi}}{q} \left[\frac{N_a}{N_d} \right] \left[\frac{1}{N_a + N_d} \right] \right\}^{1/2}$$
(16)

$$x_p = \left\{ \frac{2\epsilon_s V_{bi}}{q} \left[\frac{N_d}{N_a} \right] \left[\frac{1}{N_a + N_d} \right] \right\}^{1/2}$$
(17)

where x_n , x_p are the junction depletion widths in n and p region respectively.

The total depletion width, W is the sum of these two depletion widths and can be written as,

$$W = x_n + x_p \tag{18}$$

$$W = \left\{ \frac{2\epsilon_s V_{bi}}{q} \left[\frac{N_a + N_d}{N_a N_d} \right] \right\}^{1/2}$$
(19)

Based on above equations, the simulation model can easily be formulated to extract the electrical behaviour of a device for a specific set of inputs. The next section describes the discretization process of a second order equation through FEM.

III. FINITE-ELEMENT METHOD DISCRETIZATION

The discretization process of FEM works by dividing the whole domain (geometry) of a device into a large number of finite small elements using linear basis (or shape) functions [7], [14]. It can also be interpreted as creating large number of local domains from one global domain. Then solution of the function is evaluated over these local domains to approximate the global solution. This way, an infinite dimension problem is converted into a finite dimension problem, which can easily be represented in the form of matrix using the concept of basis functions and solved by means of any direct or iterative solvers. Any geometrically simple linear element can be taken as the basis function such as triangle, tetrahedrons, rectangular, cubes, hexahedrons etc. One such basis function of the form tetrahedron is as shown in Figure 2. These basis functions must depend linearly on x, y, zcoordinates, and are also defined in such a way that it has a defined value of "1" for mesh node j (with coordinates as $\vec{p_i} = \{x_i, y_i, z_i\}^T$ and has "0" value for all other mesh nodes. It can be represented as:

$$N_{i} = \frac{1}{6V}(a_{i} + b_{i}x + c_{i}y + d_{i}z)$$
(20)

where V is the volume of tetrahedral element

$$N_i(x_j, y_j, z_j) = \begin{cases} 1 & \text{for } i = j \\ 0 & \text{for } i \neq j \end{cases}$$
(21)

These elements must span the entire geometry in such a way that there exist no empty spaces in-between them without any overlap. Accuracy of approximated final solution depends on size as well as on number of finite elements in the discretized domain [7].



Figure 2. A tetrahedron shape function to be used as an element in FEM

The FEM is usually implemented using continuous Galerkin method of weighted residuals [7]. Galerkin method describes the finite-dimensional approximation of an infinite-dimensional space, in which a non-linear continuous function is termed as *strong form* and it is later converted to *weak form*. Weak form can be interpreted as the same function for each basic element and the complete solution of function is approximated by integrating it over whole domain. The set of governing PDEs with boundary conditions is called the strong form of the problem [7]. Here an example of a second order PDE (1D Poisson's Equation) is discussed to discretize using FEM.

$$\frac{d^2u}{dx^2} = p_0 - Strongform \qquad (22)$$

$$\frac{d^2u}{dx^2} - p_0 = 0 \quad - Residual form \tag{23}$$

$$\int_{0}^{L} \left(\frac{d^{2}u}{dx^{2}} - p_{0}\right) v dx = 0 \qquad -Weak form \qquad (24)$$

The weak form is a variational statement of the problem, which is integrated against a test function.

$$\int_{0}^{L} \frac{d^{2}u}{dx^{2}} v dx = \int_{0}^{L} p_{0} v dx$$
 (25)

Integrate LHS by parts:

-0

$$= -\int_0^L \frac{du}{dx} \frac{dv}{dx} dx + \left[v(L)\frac{du}{dx}\right]_{x=0}^{x=L}$$
(26)

$$= -\int_{0}^{L} \frac{du}{dx} \frac{dv}{dx} dx + v(L) \frac{du}{dx}|_{x=L} - v(0) \frac{du}{dx}|_{x=0}$$
(27)

Now problem is solved locally on each element.

Considering Finite basis function as $\{\varphi_i\}_{i=i}^N$, we know:

$$u(x) = \sum_{j=1}^{N} c_j \varphi_j(x), \qquad (28)$$

$$v(x) = \sum_{j=1}^{N} b_j \varphi_j(x), \qquad (29)$$

Inserting this into our weak form will give us:

$$\int_{0}^{L} \sum_{j=1}^{N} c_j \frac{d\varphi_j}{dx}(x) \sum_{i=1}^{N} b_i \frac{d\varphi_i}{dx}(x) \, dx = \int_{0}^{L} p_0 \sum_{j=1}^{N} b_j \varphi_j(x) \, dx$$
(30)

Rearranging it will give us:

$$\sum_{i=1}^{N} b_i \sum_{j=1}^{N} c_j \int_0^L \frac{d\varphi_j}{dx} \frac{d\varphi_i}{dx} dx = \sum_{i=1}^{N} b_i \int_0^L p_0 \varphi_i dx \quad (31)$$

Cancelling a term:

$$\sum_{j=1}^{N} c_j \int_0^L \frac{d\varphi_j}{dx} \frac{d\varphi_i}{dx} dx = \int_0^L p_0 \varphi_i dx$$
(32)

This gives us a matrix problem Kc = F, where K is a symmetric matrix and c is vector of unknowns, the solution

of which can be easily found using matrix solvers.

$$K_{ij} = \int_0^L \frac{d\varphi_j}{dx} \frac{d\varphi_i}{dx} dx \tag{33}$$

$$F_i = \int_0^L p_0 \varphi_i \, dx \tag{34}$$

In this section discretization process of a PDE using FEM is covered, the next section presents implementation details of the framework and results obtained for different semiconductor devices.

IV. IMPLEMENTATION DETAILS AND SIMULATION RESULTS

An efficient and parallelized framework to simulate semiconductor devices is build using finite element discretization method, capable of handling 2D/3D device geometry. The implementation details and simulation results for different devices using our simulator are discussed in this section. PDEs from classical drift-diffusion model are incorporated in the simulator, and discretized using FEM. The whole geometry is discretized into small discrete elements, which give the nodal points to solve the PDE locally. The simulator has the flexibility to select elements of different size and shape. Triangular elements have been used to discretize a 2D geometry, where as the 3D geometry uses tetrahedral elements. This leads to the formation of a mesh like structure through out the geometry in such a way that no two elements overlap each other. The simulator is capable of generating both uniform and non-uniform meshes. The use of nonuniform mesh at specific places helps to get more accurate results. This also helps to save a lot of simulation time with respect to a uniform denser mesh. The parallelization in simulator has also been achieved during the assembly process of FEM, where a bigger matrix (stiffness matrix) for all the nodes in a geometry is made from the local matrices of each element. We have used OpenMP to parallelize the assembly process, and a speedup of 1.5x has been achieved.

To showcase the effectiveness of our proposed simulator, the results for a PN junction diode and a MOS capacitor are validated with TCAD device simulator Sentaurus. The simulations curves and profiles obtained for specific device parameters and geometry are presented as follows.

A. PN Junction Diode

We have selected silicon as device material and other related device parameters used for the simulation of a pn junction diode are listed in Table I. The uniform and nonuniform meshes created by the simulator for a pn junction diode are shown in Figure 3(a) and Figure 3(b) respectively. Mesh is made more finer near the junction (depletion region) to get more accurate results. Figure 4 shows the potential profile of a diode at thermal equilibrium without applying any bias voltage. It can also be seen from Figure 4 that the built-in potential of a diode is 0.65V. The electric field

 Table I

 Device parameters and their values for a pn junction diode.



Figure 3. (a) Uniform mesh over pn junction diode (b) Non-uniform mesh over pn junction diode

inside a diode at thermal equilibrium is shown in Figure 5 and it can be seen that the electric field is present only at the junction, zero elsewhere.



Figure 4. Potential profile of a 2D pn junction diode at equilibrium

The total current density for a forward bias voltage across a diode, as simulated by the simulator is shown in Figure 6. It can be seen that diode remains OFF (cut-off region) as long as the applied voltage is under built-in potential barrier, and the diode gets ON once it crosses the barrier.

A 3D structured pn junction diode is also simulated for same device parameters with non-uniform meshing using tetrahedral elements throughout the volume of the device as shown in Figure 7. The potential profile for this 3D diode is shown in Figure 8.



Figure 5. Electric filed inside a pn diode at equilibrium



Figure 6. I-V characteristic of a forward bias pn junction diode



Figure 7. Non-uniform meshing for a 3D pn junction diode

B. MOS Capacitor

A 3D MOS capacitor is also simulated with the simulator using device parameters listed in Table II. Figure 9 shows the potential profile inside a MOS structure when gate is supplied with positive voltage.

The simulations performed validates the working of our simulator for 2D/3D geometries using FEM as the discretization method.



Figure 8. Potential profile of a 3D pn junction diode at equilibrium

Table II Device parameters and their values for a 3D MOS capacitor.

Device parameters	Value
Device dimensions: Width, Depth	$180 \ nm$
Oxide material	SiO_2
Temperature: T	300 K

V. CONCLUSION

In this paper, we have presented a parallel 2D/3D device simulator for semiconductor devices, which uses finite element method to discretize several partial differential equations. The simulator has employed the classical driftdiffusion model to implement various fundamental device equations. The simulator is capable of producing uniform and non-uniform mesh through out the geometry. Having denser mesh only at specific places helps us save a lot of simulation time with respect to a uniform denser mesh. To validate the working and efficiency of our simulator we have simulated a PN junction diode for both 2D and 3D geometry, and a 3D MOS capacitor. The potential profile, electric field and total current density have been shown in results. We have also been able to achieve parallelization in simulation, during the assemble process of the FEM, and successfully achieved 1.5x speed up. Having validated the working of our simulator with drift-diffusion model using FEM for different device geometries, we will extend the work to simulate more novel devices like FinFET, GAAFET etc. Although there are many commercial TCAD device simulator available to study and design semiconductor devices, the purpose to build a FEM based model is to develop a platform for quicker, more efficient and accurate novel device designs. This will help us not only to increase the speed of analysis of device equations in a reasonable time, but also to explore different methodology to be used to produce semiconductor device models. As we know there are many design corners at which device model fails to produce desired solution, a more accurate solution will enable us to develop a better model for reliable circuit design using novel devices. In this paper



Figure 9. Potential profile inside a 3D MOS capacitor

pn junction diode and MOS capacitor are designed using developed simulator and the results have been validated with TCAD device simulator Sentaurus.

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