A Primer for Mapping Techniques on NoC Systems

M. Sacanamboy[1], F. Bolaños[2], and R. Nieto[3]

[1]Department of Electronics and Computer Sciences, Pontificia Universidad Javeriana, Cali, Valle del Cauca, Colombia

[2]Department of Electrical Engineering and Automatics, Universidad Nacional de Colombia, Medellín, Antioquia, Colombia

[3]Department of Electrical Engineering, Universidad del Valle, Cali, Valle del Cauca, Colombia

Abstract - *This paper is aimed to present a detailed description of the main factors which must be considered for task mapping onto Network on Chip (NoC) systems. A survey of the most representative and outstanding reported works is presented, along with conclusions and future work regarding such a review.*

Keywords: NoC (Network on Chip) Systems, Task mapping.

1 Introduction

In order to cope with performance requirements imposed by applications, current computing systems are moving to multicore platforms. Among such high performance systems, embedded systems represent a big fraction of the market, involving a plethora of devices such as portable devices, vehicles, wireless sensors, home devices, and so on.

Embedded systems are designed to implement special features, and are different from generic computing systems in the fact that they are devoted to implement one or more specific functionalities. Such systems are constrained by the applications, which impose operating conditions related to some figures of merit, such as performance, real time, power consumption, cost, etc. In order to cope with such constraints, designers have conceived systems with several processing cores, which may be different from each other, and are organized on a single chip (MPSoC) [1, 2].

Heterogeneity in current MPSoC systems is related with the variety of features which are present on each system core, and allows achieving flexibility in dealing with several kinds of applications. Many of current research efforts rely on improving the interconnection and synchronization systems of such cores, for the sake of speeding up the overall performance of the system. Interconnection buses are running out of capacity when dealing with a larger number of nodes inside the system, so it is mandatory to conceive efficient and structured communication architectures for these MPSoC systems [3].

NoC systems are a current approach aimed to achieving such interconnection objectives. Among some of its appealing features, the use of NoCs is preferred because of their scalability, high performance, and modularity. Particularly, by using NoC systems it is possible to achieve concurrent communications, as well as high components reusability.

NoC systems are composed of nodes and a communication architecture, which is based on network interfaces (NIs) and routers. Routers are plugged to communication channels, and nodes access such resources by means of the NIs. Nodes are often related to computational or storage resources, or a combination of both.

One of the most critical stages in designing a current embedded system is the mapping of tasks onto the available resources of the NoC. Such stage depends on the application, as well as the target NoC architecture. Some factors which are related to such an important design stage are [4]: Application constraints, figures of merit for system optimization, available mapping tools and their limitations, available information of the system. Because of all of these issues, task mapping is classified as a hard NP–problem [5].

This work is aimed to present a first review of several factors which are involved with task mapping methodologies in NoC systems. The paper is organized as follows: Section 2 summarizes the key factors which must be taken into account in the task mapping stage for NoC systems. Section 3 surveys some of the most representative works on this issue. Conclusions and future work are presented on Section 4.

2 Key factors on task mapping

Due to its criticity, some key factors must be considered in the stage of mapping of tasks onto a NoC system. Such key factors are described below.

2.1 Target architecture

The target architecture is related to whether nodes on the NoC system are heterogeneous or homogeneous.

Heterogeneity is the most common case, because this factor may improve system performance in presence of different kinds of applications. Heterogeneity refers to having several kinds of nodes in the system (i.e., nodes may be different among them).

2.2 Abstraction level of the application specification

The abstraction level in which applications are described is a key factor in mapping tasks of such applications to the available resources. The first possible approach on this subject is to use Register Transfer Level, or RTL. RTL is a valuable tool for modeling and designing complex systems, and often relies on hardware description languages, such as VHDL (VHSIC Hardware Description Language) and Verilog. Such tools allow modeling a part of the NoC system such as the communication system, or even the entire system [6].

The second reported approach is based on transaction-level modeling or TLM. Transactions are defined as the event of synchronization or data exchange among system modules. This approach is appealing because it allows performing a functional verification of the system, and the modeling is based on languages such as SystemC [7]. TLM has been used successfully for synthesizing high speed MPSoC systems [8], and for modeling the communications infrastructure of a NoC [9].

2.3 Figures of merit

This factor refers to the optimization criteria which must be considered along the optimization process related to the mapping stage. Such optimization can be viewed as a solutions space exploration, where each solution represents a single design choice with different values for the objective functions. The task mapping process must find an acceptable solution within the space with allowable and optimized values for such functions. Among the most common figures of merit used for such optimization process, we may find: power consumption, delay time, mapping time, temperature, mean number of hops across the network, network contention, mean channel occupancy, bandwidth, and so on.

2.4 Common–domain semantic

This is a medium level representation which combines information both from the high level application description and from the implementation platform. Among the plethora of representations available for these purposes, graph-based approaches are the most common, with instances such as task graphs (TG), communication task graphs (CTG), communication weight graphs (CWG), communication resources graph (CRG), annotated task graphs (ATG),

synchronous and asynchronous data flow graphs (SDFG and ADFG), and so on. Some other kinds of such medium–level representation are the Petri Networks (PN), and the Kahn Process Networks (KPN).

2.5 Topologies

Topology refers to the way in which system nodes are physically interconnected. Topologies may be classified as either regular or irregular. Some instances of common topologies are meshes, torus, rings, and spidergon ones. Regular topologies are more constrained with respect to the connections distribution, which are generated by means of mathematical functions [2, 17]. Irregular Topologies are often the mixture of two or more regular forms, which leads to hybrid, hierarchical or totally irregular topologies.

2.6 Optimization algorithms

As already mentioned, the mapping stage relies on an optimization process, which searches along a solutions space, the design with a better tradeoff among the chosen figures of merit. The kind of optimization algorithm used for task mapping has a direct impact in the communications nature [10]. For instance, off–line (static) optimization forces to having predictable communication assessments, whilst dynamic algorithms allow a more flexible communication scheme.

A subset of static algorithms encompasses the so called exact approaches, which are based on mathematical modeling of the optimization problem. Integer Linear Programming (ILP), Non Integer Linear Programming, and Mixed Integer Linear Programing, are well–known instances of exact algorithms, but their drawback relies on their poor convergence performances as the problem size increases [12].

On the other hand, search–based techniques are divided in heuristic and deterministic algorithms. Deterministic algorithms are devoted to search along the whole solution space, whereas heuristic algorithms use the previous experience in order to improve the searching process. Among heuristic algorithms there are some approaches which work with evolutive techniques (transformative) and some others which produce partial solutions in an iterative fashion until a good–enough solution has been reached (constructive). Dynamic algorithms are all based on heuristics. They must be quick enough to deliver a reasonably good solution in run time, without sacrificing task mapping quality. Table 1 summarizes the taxonomy above described.

Table 1. Taxonomy of the Optimization Algorithms.

Algorithm	Nature	Kind
First Free (FF)	Dynamic	Heuristic
Nearest Neighbor (NN)		
Packing-based Nearest Neighbor (PNN)		
Minimum Maximum Channel Load (MMC), Minimum Average Channel Load (MAC)		
Path Load (PL)		
Best Neighbor (BN)		
Dynamic Spiral Mapping (DSM)		
Lower Energy Consumption based on Dependencies-Neighbor (LEC-DN)		
ILP, NILP, MILP	Static	Exact
Genetic Algorithm, Particle Swarm Optimization, Ant Colony Organization, Population-Based Incremental Learning	Static	Heuristic – Transformative
Binomial, Mapping Algorithm, Constructive Mapping Algorithm, Chain Mapping Algorithm, Mapping on Noc, Simulation Environment Mapping, LMAP Algorithm, Simulated Annealing, Onyx, Search Tabu	Static	Heuristic – Constructive
Branch and Bound	Static	Deterministic

2.7 Tools

Some software tools are available for supporting the task mapping stage in NoC design environments. Among such tools the following can be mentioned below.

• SUNMAP selects the best topology according to application constraints (power, bandwidth, communication delay) and generates the nodes allocation for the target application and architecture. The process involves three steps. Firstly, routing algorithm and allocation objectives must be selected. In second place, the best topology is chosen and thirdly, a model of the system is provided through SystemC descriptions [13].

• SMAP is a mapping and simulation tool developed in the Matlab environment, which provides several optimization choices for the solution space exploration. Some of these options are Genetic Algorithms, random, and spiral. The communication among nodes can be simulated with both deterministic routing algorithms (such as XY) or adaptive algorithms (such as west-first or backtracking). Some figures of merit assessments, such as power consumption or execution time, are provided by the tool [14].

• HeMPS is a custom platform for design and simulation of NoC-based MPSoCs. This tool is based on the Hermes network, a Noc with a two dimensional mesh topology, a XY routing algorithm, and a wormhole commutation mode. Nodes in Hermes may be a MIPS processor, a RAM memory module, a DNA module, or a NI module. First design stage in HeMPS implies identifying the application specifications and constraints. After that, some hardware platform parameters (such as the size of the network, packet size, memory size, etc.) must be settled and the partitioning algorithm is able to start. The last stage implies the task mapping of the application on the selected platform. Both static and dynamic mapping is supported. The designer is able to integrate hardware and software components to perform a simulation and validation of the whole system. The final stage generates a description of the platform by means of a Hardware Description Language (HDL) [15].

• OPNEC is an open code platform for designing and simulating NoC systems. It supports a variety of 2D and 3D NoC architectures and several topologies (mesh, torus, ring, bus). It is also capable of working with both static XY routing algorithms and adaptive approaches, and supports several kinds of processor and memory modules. Several optimization objectives might be used, such as energy consumption and communication delay. Energy assessments are achieved by means of RTL models and are aimed to provide estimations of the whole network system.

Table 2. Summary of reported mapping solutions

Ref.	Factor		
	Optimization Criterion (Figures of Merit)	*Common Domain Semantic / Optimization Algorithm*	*Target Architecture and Abstraction Level*
[18]	Execution time	CTG / Exact optimization	Homogeneous architectures and Algorithm abstraction
[19]	Energy Consumption	CTG / Heuristic Constructive	
[20]	Energy Consumption	TG / Exact optimization	Heterogeneous architecture and Algorithm abstraction
[21]	Communica-tion cost	APCG / Heuristic Transformative	
[22]	Communica-tion volume	CTG / Heuristic Transformative	
[23]	Multi-objective	TG / Heuristic Transformative	
[24]	Bandwidth, Area	CTG / Heuristic Constructive	
[25]	Energy Consumption, Latency	ARG / Heuristic Constructive	
[26]	Communica-tion Cost, Bandwidth	CG / Heuristic Constructive	Heterogeneous architecture and TLM abstraction
[27]	Execution Time	AG / Dynamic	
[28]	Execution Time Energy Consumption, Average channel load, Latency	AG / Dynamic Optimization	
[29]	Energy Consumption	CTG / Dynamic optimization	Heterogeneous architecture and RTL abstraction
[30]	Execution Time	SDFG / Heuristic Transformative	
[31]	Energy Consumption, Execution Time	CWG, CRG / Heuristic Constructive Dynamic	Homogeneous architecture and RTL abstraction

3 Reported mapping solutions

This section summarizes the most representative reported works in the subject of mapping solutions aimed to NoC systems. In order to efficiently present such information, Table 2 relates some of the literature references, with some key factors on task mapping, as described in Section 2. Some abbreviations are used in Table 2. Their meaning is as follows. CTG: Communication Task Graph; TG: Task Graph; APCG: Application Characteristics Graph; CG: Core Graph; AG: Acyclic Graph; SDFG: Synchronous Dataflow Graph; CWG: Communication Weights Graph; CRG: Communication Resources Graph.

In Table 2, all reported solutions work with mesh topologies with exception of reference [30]. None of them is aimed to hierarchical, hybrid, or irregular topologies.

4 Conclusions

This document introduces a brief summary on task mapping techniques for NoC Systems. A taxonomy of key factors involving task mapping methodologies is introduced. Finally, a survey of reported works in literature, regarding tasks mapping is also presented. This survey includes some of the key factors previously presented.

According with the results summarized in Table 2, most of the mapping solutions reported in literature are aimed to mesh NoC topologies. Network regularity and ease of simulation and implementation might be part of the reasons why mesh topologies are preferred. As future work, we devise the study of mapping solutions in hierarchical and more complex network topologies.

5 Acknowledgements

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