FPGA Synthesis of Glucose-Insulin Feedback System

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Abstract—**Goal of this paper is to develop a hardware realization of Insulin-Glucose feedback system based on FPGA. Behavioral modeling of the mechanism is developed with the aid of Hardware Description Language(HDL). Digital Differential Analyzer (DDA) algorithm is used in order to solve the mathematical model of insulin glucose dynamics. The simulation is synthesized using Xilinx Design Suite (9.1i) and downloaded into a Combinational Complex Programmable Logic Device (CPLD) / Field Programmable Gate Array (FPGA) Xilinx XSA-50 microchip.**

***Keywords*—Insulin-Glucose feedback system, FPGA synthesis, Digital Differential Analyzer, Pulsatile Insulin.**

I. INTRODUCTION

As with the design of any compound engineering system, realistic computer simulation can provide vital information about the safety and confines of algorithms, can guide and focus the emphasis of clinical studies, and can out-rule unrealistic scenarios in a cost-effective manner prior to human use. In the area of diabetes, accurate computer-simulation prediction of clinical trials has been done by the Archimedes diabetes model [1, 2]; a company—Entelos Inc. specializes in predictive bio simulation and in particular has developed a diabetes simulator. The ability of recent diabetes simulators are narrowed to prediction of average population that would be observed during clinical trials because these simulators are based on population models. For this reason a different kind of computer based simulator is needed in order to realize the function of artificial pancreas which should be capable of simulating the glucose–insulin dynamics of an individual. Various glucose–insulin models [6], [7-9] have been developed to serve this purpose.

In the glucose–insulin endocrine metabolic regulatory system, the two pancreatic endocrine hormones, insulin and glucagon, are the primary regulatory factors. Numerous in vivo and in vitro experiments have revealed that insulin secretion consists of two oscillations occurring with different time scales: rapid oscillations having a period of 5–15 min [10] and ultradian oscillations occurring in the period of every 50–150 min [11-13]. Considerable amount of work has been done in the field of biological simulation. Botros et al modeled biological mechanism such as human growth hormone secretion and simulated it using FPGA [3- 5].

In this paper we synthesize the glucose-insulin model developed by Tolic et al. The FPGA chip is tested by comparing its output with that of the afore mentioned paper [tolic]. In the paper Tolic et al developed a set of differential equations which can successfully describe the glucose – insulin feedback system. Solving these differential equations in a digital environment is a challenge because digital computing has also its limitations. Thus, recently some researchers are exploring ways to return to the use of the analog computing method again [14], especially in cases where ultrafast speed of the solving process is needed (real-time simulation).

II. MATHEMATICAL MODEL OF GLUCOSE – INSULIN MECHANISM

Numerous in-vivo and in-vitro experiments have shown that insulin concentration oscillates in two different time scales: rapid oscillation with a period of 5-15 minutes and ultradian oscillation with a range of 80-150 minutes ([11], [10], [13] and [15]).Ultradian oscillations of insulin concentration are believed to be mainly due to glucose interaction in the plasma and instability in the insulin-glucose feedback system([11], [12], [13] and [16]).

To determine whether the ultradian oscillations could result from the interaction between insulin and glucose, a parsimonious nonlinear mathematical model consisting the six ordinary differential equations including the major mechanisms involved in glucose regulation was developed by J. Sturis, K. S. Polonsky, E.Mosekilde and E. Van Cauter ([11]) in 1991 and recently simplified by I. M. Tolic, E. Mosekilde and J. Sturis ([12]) in 2000. The purpose of these two models was to provide a possible mechanism for the origin of the ultradian insulin secretion oscillations.

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The simplified model takes the form:

$$\frac{dI_p}{dt} = aI_p + bI_i + cG + d \qquad (1)$$

$$\frac{dI_i}{dt} = eI_p + fI_i \quad (2)$$

$$\frac{dG}{dt} = gI_iG + hG + kx_3 + p \qquad (3)$$

$$\frac{dx_1}{dt} = r\left(I_p - x_1\right) (4)$$

$$\frac{dx_2}{dt} = r(x_1 - x_2) (5)$$

$$\frac{dx_3}{dt} = r(x_2 - x_3) (6)$$

The model has three main variables: the amount of glucose in the plasma and intercellular space, *G*, the amount of insulin in the plasma, I_p ,and the amount of insulin in the intercellular space, I_i. In addition, there are three variables x_1, x_2 and x_3 that represent the delay between insulin in plasma and its effect on the hepatic glucose production.
Values of the parameters *a,b,c,d,e,f,g,h,k,p,r* are taken from the paper [9].

III. FPGA IMPLEMENTATION AND ARCHITECTURE

In order to synthesize the glucose – insulin system using FPGA, Digital Differential Analyzer (DDA) algorithm is used to write the Hardware Description Language (HDL).
A digital differential analyzer (DDA), also sometimes called "digital integrating computer", is a digital implementation of the differential analyzer. The integrators in DDA are implemented as accumulators, whereby the numeric results are converted back to a pulse rate by the overflow of the accumulator. The main advantage of the digital integrator, when compared to an analog integrator, is the scalable precision. Also, in a digital integrator based on DDA, we don't have drift errors and noise [17] due to the imperfection of electronic components. By accumulation over time of values in a register we can calculate the integral of signals. The basic digital integrator is expressed by (7).

$$V_{n+1} = V_n + K.S \qquad (7)$$

In (7),*Vn*+1 denotes the next state of the accumulator used for calculating the integral. The coefficient of *K* is a constant factor that is less than 1; it is used for time scaling. In this equation *S* denotes the input signal for integration. We can map this technique on FPGA very easily by writing a behavioral code. After each rising clock pulse, the equation updates the integral value. In this integrator, Rounding or truncation errors are only due to the limitation of registers.
Fig 1 shows the architecture of the DDA based differential equation solver which is downloadable to the FPGA chip.
The multiply is replaced by a shift-right as `dt` is chosen to be a power of two.

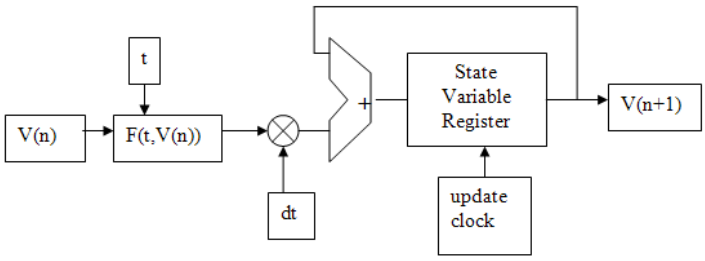

Fig 1: Hardware architecture of Digital Differential Analyzer

We can rewrite equations (1) – (6) by applying DDA as follows:

$$I_{p(n+1)} = I_{p(n)} + \left(aI_{p(n)} + bI_{i(n)} + cG(n) + d\right) \times dt \quad (8)$$

$$I_{i(n+1)} = I_{i(n)} + \left(eI_{p(n)} + fI_{i(n)}\right) \times dt \qquad (9)$$

$$G(n+1) = G(n) + \left(gI_{i(n)}G(n) + hG(n) + kx_3(n) + p\right) \times dt \qquad (10)$$

$$x_1(n+1) = x_1(n) + r\left(I_{p(n)} - x_1(n)\right) \times dt \qquad (11)$$

$$x_2(n+1) = x_2(n) + r(x_1(n) - x_2(n)) \times dt \qquad (12)$$

$$x_{3(n+1)} = x_{3(n)} + r\left(x_{2(n)} - x_{3(n)}\right) \times dt \qquad (13)$$

IV. EXPERIMENTAL RESULTS

The FPGA technology provides a programmable interface to enable us to synthesize complex behavior models. FPGA chips Configurable Logic Blocks (CLBs) can be personalized to represent different models. The three distinguishing features of FPGAs chip: ***architecture, function-unit granularity and intra/inter-chip wiring organization*** can be fine-tuned to represent complex models in a fairly short period of time. Combined with HDL tools, we have a powerful tool to represent and synthesize the mathematical model.
In this experiment we used Xilinx ISE design suit 9.1i and the XSA-50 board which is equipped with *SPARTAN-2* type FPGA. The inbuilt clock signal is used to perform the experiment in a real time environment.
The steps of the experiment are shown in the Fig. 2 and Table 1 shows the numerical values of glucose and insulin after FPGA synthesis.

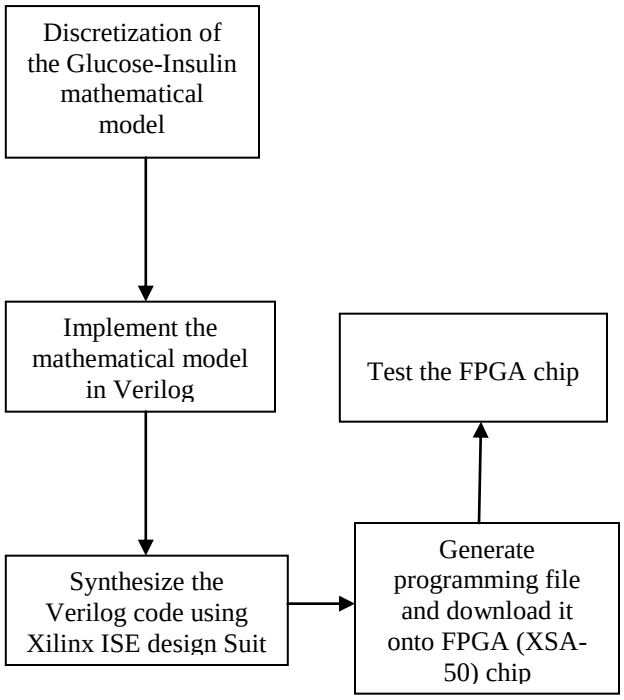

Fig 2. Implementation of the mathematical model onto the FPGA chip.

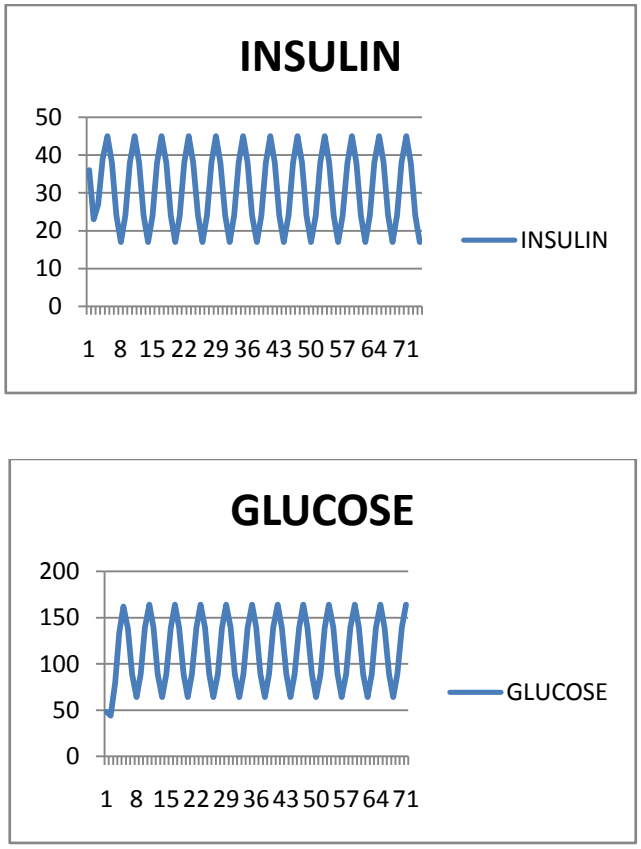

Fig 3. FPGA output of the Glucose Insulin feedback system

TABLE 1. Numerical values of glucose and insulin

TIME	INSULIN (Mg/dl)	GLUCOSE (Mg/dl)
1	36	48
2	23	44
3	27	79
4	39	134
5	45	162
6	38	138
7	24	89
8	17	64
9	24	89
10	38	139
11	45	164
12	38	139
13	24	89
14	17	64
15	24	89
16	38	139
17	45	164
18	38	139
19	24	89
20	17	64
21	24	89
22	38	139
23	45	164
24	38	139
25	24	89
26	17	64
27	24	89
28	38	139
29	45	164
30	38	139
31	24	89
32	17	64
33	24	89
34	38	139
35	45	164
36	38	139
37	24	89

Fig 3.illustrates the numerical values of Glucose and Insulin. We used Microsoft excel in order to visualize the glucose insulin oscillations as described in the paper [9].

TABLE 2. Resources used by FPGA

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	48	768	6%
Number of Slice Flip Flops	32	1536	2%
Number of 4 input LUTs	83	1536	5%
Number of bonded IOBs	9	92	9%
Number of GCLKs	1	4	25%

The number of resources used after synthesis for solving the Gluocse Insulin dynamical equations, Flip-Flop slices and 4-Input LUT Slices are shown in the Table 2.

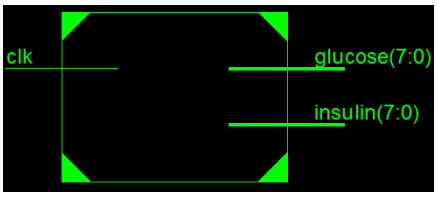

Fig 4. The RTL Technology schematic

Fig 4. Illustrates the chip developed by the Xilinx ISE design suite. The input is the clock signal and output is the glucose and insulin signals. Each of them is 8 bits wide.

The following figure shows the input clock signal and the output Glucose and Insulin signal after simulation using the Isim simulator provided by Xilinx ISE .

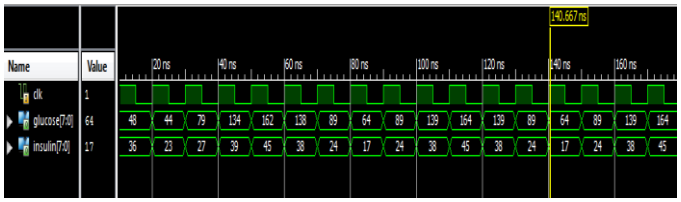

Fig 5.Isim simulation output of the Glucose Insulin feedback Model.

V. FUTURE WORK

In this paper we synthesized a constant glucose insulin feedback system. It is possible to see the response of insulin after meal injection or random glucose input. From hardware design perspective, generating the HDL code for solving dynamic equations by a flow diagram can be done in future. For modeling a complex system the future program will be node-based. After coupling nodes by either code or a GUI, the program will be able to generate a gate level HDL code for direct programming on FPGA. By this technique we can speedup the design and implementation process of analog computing solvers on FPGA, which will be capable of solving complex differential equations and simulating complex systems in real time on FPGA.

VI. CONCLUSION

We have used a previously successful mathematical model that describes the Glucose - Insulin feedback system patterns in humans to generate a blueprint for a microchip and generated a bit file to the prototyping board and produced some simulated hormone level figures from the chip. The result shows that the FPGA chip can successfully mimic the ultradian oscillation as described in the paper [12]. In future this research can lead us to develop a pocket friendly easy to maintain insulin pump which can secret insulin based on the meal injection in a purely digital environment.

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