Software-Based Reconfigurable Computing Platform (AppSTAR™) for Multi-Mission Payloads in Spaceborne and Near-Space Vehicles

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Abstract—We present an on-demand rapidly reconfigurable (~seconds) software-defined payload (SDP) architecture called AppSTAR™ with a core in-situ re-programmable processing capability that supports communications, radar, signal analysis and other missions. At the heart of Harris' AppSTAR™ SDP concept is a Virtex-based FPGA and interconnect fabric architecture that provides for a modular, flexible, scalable core capable of supporting a broad spectrum of missions with capabilities that can be customized for size, weight and power (SWaP) challenged platforms. Illustrating some of the capabilities evolving from this work, we present two real-world space qualified/qualifable SDPs, 1) a 100 Mbps-capable Ka-band software defined radio (SDR) for NASA and 2) a space-ready SAR/ISAR X-band RADAR based on the AppSTAR™ core. We also present an application of this core in a payload for an reconfigurable multi-mission space payload. The work described herein primarily leverages our space qualified V4 Processor employing several FPGAs in excess of 1 million gates each. Related work offering dramatically increased integration, reducing the V4 Processor card to 1 cubic inch package suitable SWaP challenged near-space and terrestrial applications is also discussed.

I. INTRODUCTION

Software defined radios (SDRs) have gained popularity due to the rapid reconfigurability of devices enabling the radio system to dynamically adapt to varying operational scenarios during a deployment or mission. Modern adaptation techniques include autonomous [1, 2] or cognitive methods [3], while traditional methods require external intervention (e.g. user entry or network control). Regardless of the adaptation method, the clear benefit is a single hardware platform that provides robust services over varying channel conditions and network connectivity, for example via adaptive modulation and/or waveform selection [4]. A key to the versatility of the SDR is that it relies on programmable computational hardware resources (e.g. DSP processors, FPGAs) rather than the dedicated circuitry typical in limited function MODEMS. A further attractiveness of SDRs is that they can be efficiently implemented using a high performance computing engine. Further, the commonality of the engine to support a spectrum of applications requiring advanced signal processing is supportable using a common tool suite and interfaces that enables dramatically lower non-recurring engineering costs, dramatically shortens development cycles, and improves the overall life cycle costs. This paradigm has been exploited in the development and real-world application Harris' V4 Reconfigurable Space Processor (V4 RSP) and highly integrated version the SiP-100 in the AppSTAR™ strategy.

The application of software-based dynamically reconfigurable DSP technology in the satellite domain has been limited. This is due to a number of interrelated factors such as

- space environment survivability
- limited SWaP envelope
- reconfiguration requirements
- software deployment/management complexity

However, it is possible to overcome these barriers and provide a highly flexible capability using an in-situ dynamically programmable hardware core (figure 1-1) we term the software-defined payload (SDP) AppSTAR™ concept which is a more general view than an SDR.

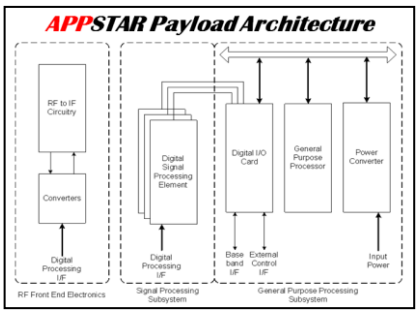

Figure 1-1: Software defined payload block diagram.

An SDR is a specialized case of adapting just one sub-system of a typical multifunction payload. The SDP on the other hand, is a concept where the "personality" and capabilities of a payload are quickly (~ seconds), and possibly autonomously, reconfigured on-orbit (figure 1-2) to meet subscriber service demands or a changing business model for commercial/civil space in remote sensing and communication.

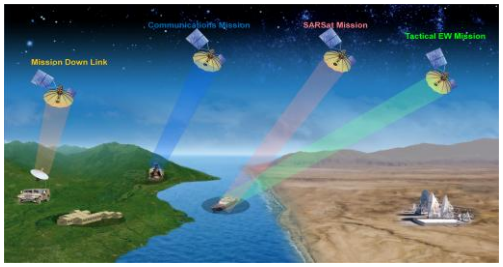

Figure 1-2: Notional use case for reconfigurable payload

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This paper presents current work on a space qualified multi-mission payload compute-engine supporting the SDP concept based on an FPGA hardware architecture that supports complete or partial in-situ on-demand reconfiguration of the processing elements. We chose FPGAs as the computing platform to achieve a balance in the cost, power, performance trade-space between ASICs and fully programmable processors. Our approach utilizes advances in radio management software, signal processing hardware, and adaptable systems to meet not only radio systems needs, but those of other missions as well such as signal collection/processing, communication, RF imagery remote sensing (i.e. SAR/ISAR) and could be extended to other missions such as MOVINT (e.g. GMTI). The paper will also present the capability of the hardware elements operating in various sensor and communication instantiations for real-world applications.

The paper is organized as follows. Section II discusses SDP concept (section II.1) and two hardware variants of the same core, the V4 processing element (section II.2) and SiP-100. We also present some of the issues and mitigations for a reconfigurable spaceborne platform for operation and survivability in various radiation environments (section II.3). Sections III and IV present application of the V4 Space Processor in a communication payload and a remote sensing payload. Assuming the existence of various RF support elements, the applications could be melded into a single payload. Presently we leverage the reconfigurability of the hardware platform by merely loading different application software/firmware to customize the processing resources to the target application. The paper concludes with some closing commentary in section V.

II. FPGA-BASED SOFTWARE DEFINED PAYLOAD

II.1 AppSTAR™ SDP Concept

Harris has been delivering multi-processor based Software Defined Payloads (SDP) since 1998 resulting in a development path from general purpose RISC processor-based architectures to today's modern SDP architectures based on Xilinx Virtex FPGAs. With the advent of high performance FPGA processors, and techniques [6] which allow them to operate in space environments, the performance and reconfigurability necessary to tackle more complex processing scenarios has become increasingly viable.

The high-level block architecture of a generic AppSTAR™ SDP is illustrated in Figure 1-1. The basic elements of the system are the General Purpose Processing (GPP) Subsystem, the Signal Processing Subsystem, and the RF Front End Electronics Subsystem [6]. The GPP controls the payload operations and includes functions to load waveforms or configuration data. The GPP includes a common set of software infrastructure components that provide essential system management functions regardless of payload function through a consistent set of interfaces to configure, manage, and control the system hardware resources. The digital I/O cards provide standard interfaces to the vehicle, and can be customized for unique needs of a particular point application. The RF electronics are generally a separate package from the digital subsystems so that the RF functionality may be placed close to the aperture which tends to benefit overall system performance. The signal processing subsystem is a prime focus of this paper. The configuration of the signal processing subsystem dictates the function of the payload. This is the core of the AppSTAR™ concept.

A fundamental tenet of the Harris approach has been the incorporation of standards and leveraging commercial off the shelf (COTS) products to the greatest extent possible into the radio architecture. Operation of the Harris SDP utilizes a mix of commercial-off-the-shelf (COTS) hardware and software. A commercially available real-time operating system (RTOS) provides the key interface between the hardware and operating environment (OE). The OE is based on the NASA Space Telecommunications Radio System (STRS) infrastructure. The system backplane uses the compact Peripheral Connect Interface (cPCI) standard. As a physical interface standard, Spacewire using the Remote Memory Addressing Protocol (RMAP) is employed to provide the intra- and intercomponent communications.

In prior work, limited to SDRs, it was found that requiring knowledge of the underlying physical architecture was a significant impediment to waveform porting and third party development in FPGA implementations [7]. Therefore, a key design objective in SDP using the V4 Space Processor is to enable third party development, while ensuring that the application will not harm the hardware or other payloads on the spacecraft. To achieve these opposing objectives, a set of Hardware Description Language (HDL) modules have been designed and implemented to abstract the hardware details of the SDR and provide a standard interface for payload developers and mission planners [7, 8]. Hardware abstraction is a key aspect of developing a software radio that promotes extensibility and new application development [8]. Additional work is needed to create abstractions of processing elements representing an entire spacecraft bus that uses a single or set of SDPs in order to promote the inclusion of third parties in evolving applications for reconfigurable spacecraft. We have taken some first steps in this direction with hardware abstractions of the SDR [8]. These abstractions have led to the ability to easily use the V4 Space Processor in several remote sensing applications in addition to the communication applications it was envisioned for.

II.2 The V4 Reconfigurable Space Processor

The V4 Reconfigurable Space Processor (V4 RSP) is shown in figure 2-1 and is a core element of the SDP concept (figure 1-1) and provides a flexible compact Digital Signal Processor (DSP) module that delivers throughput rivaling dedicated ASIC-based solutions while providing an optimal balance in SWaP, cost and performance between dedicated function ASICs and fully programmable DSPs.

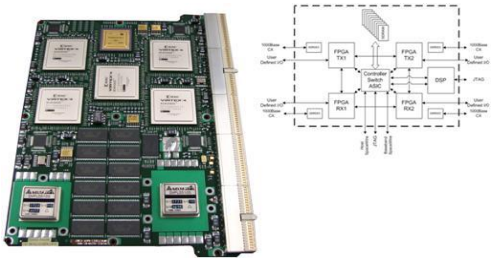

Figure 2-1: V4 RSP and block diagram.

The V4 RSP is latest variant of a line of sustained R&D into radiation resistant reconfigurable computing elements, complete with signal interfaces and data conversion, suitable for space environments. It integrates high performance Virtex-4 FPGAs (256 GOPS), 1 GLOP general purpose DSP (SMJ320C6701), 256 MB RAM, flexible standard IO (IEEE 1149.1 JTAG, Dual Spacewire, four 1000 base CX 2.5 Gbaud serial ports, and SEU Circumvention logic along with demonstrated total dose hardness > 30 Krads, into a single conductively cooled 6U compact PCI (cPCI) form factor consuming ~ 30W. The SDRAM shown is used to hold the application data, and the SDRAM is portioned amongst several possible applications (e.g. typically 16) for a mission. The SDRAM can also be reprogrammed "at will" to provide updates during a mission as warranted. Also, provisions have been made in the design such that larger fabrics of multiple processing cores can be easily woven together to form even more capable designs. Lastly, we are currently considering the system-level impacts to size, weight, power and speed of the new variants of Virtex radiation resistant/tolerant FPGAs, such as the Virtex 5Q family, as possible upgrades to our existing designs [5].

The V4 RSP has been used as a core element in several space systems research and development programs such as the NASA CoNNeCT SDR (section III) and two Imaging RADAR efforts (section IV). The V4 RSP (figure 2-1) will be undergoing in-situ testing as part of the NASA CoNNeCT SDR on the International Space Station in late 2012 (planned).

A major issue impacting the design and deployment of reconfigurable hardware in a space or near-space environment is radiation. Both prompt and long-term effects must both be considered. The V4 RSP addresses this issue by design. Elements impacting the design of this processing element are outlined in section II.3. However, for applications not requiring the radiation resistance of a space-deployable design, Harris has continued evolution of re-configurable processing engines into the highly integrated SDR SiP-100 (figure 2-2).

The SiP provides similar core functionality to that of a board-sized V4 space processor (figure 2-2), but has dramatically increased levels of integration. At a top-level, the Harris SDR SiP is composed of 25 million programmable gates over 5 FGPAs, one DaVinci DSP (which includes separate DSP and ARM-9 processors), two 125 Msps 14-bit ADCs, two 500 Msps DACs, 1 GB RAM, 1 GB Flash memory, USB 2.0 and Ethernet interfaces, an embedded operating system, on-module power management controls, and has equivalent processing capacity as a 160 GHz desktop computer. The small size and short bus lengths allow lower drive current, exhibiting low power and negligible digital noise.

The SDR SiP-100 is currently at technical readiness level (TRL) 7, having completed low-rate initial production (LRIP), passing MIL-STD-883 for 500 temperature cycles (-40°C to 100°C) and 100 g shock and vibration, and being demonstrated in multiple operational prototypes. The SDR SiP-100 is ideally suited for small systems, including man-pack, handheld, UAV's and other SWaP limited systems.

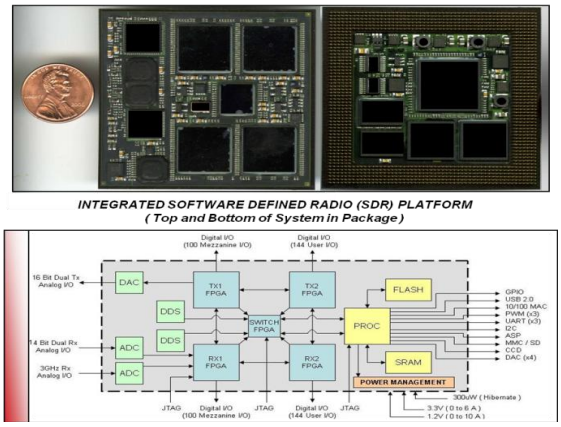

Figure 2-2: System in Package (top) & SDR diagram (bottom).

Similar to the V4, at a "flip-of-a-switch," the SDR SiP-100 can be dynamically repurposed to a new communications mode/waveform or recommit the entire computational fabric to perform functions for remote sensing or other desired operation. The FPGAs are typically loaded via the DaVinci's ARM-9 processor from on-module memory or off-chip resources.

The Harris SiP has already found use in miniature terrestrial software-defined radios [11], and is a step towards producing radios on a chip. An example of a packaged SiP-100 and tested in an SDR is shown in figure 2-3. The figure illustrates the evolution of the board-level

architecture V4-like system, into a deployable µTCA-compliant SiP-100 SDR platform.

In lab demonstrations the SiP-100 has shown that it provides high signal quality of -43 dB EVM for 64 QAM OFDM, demonstrated at over 200 Mbps [11]. Also, using the same hardware in the µTCA-compliant SiP-100 SDR platform we have implemented a novel digital chaotic communications system supporting a 100 kbps simplex link using a 10 MHz chaotically spread QPSK signal, with robust communications performance down to -13 dB below the intended receiver's noise floor. BER performance has been measured within 1 dB of theory, down to 8.5×10^{-6} [12].

The SiP provides an enabling technology for the emerging class of high altitude surveillance platforms called near-space vehicles (NSV) [13]. One potential application of low-altitude NSVs is to provide a rapidly deployable aerostat-based multi-standard cellular base station for disaster support. The dynamic reprogrammable capability of the SiP-100 enables the platform to be field reconfigured to support any of a variety of cellular or push-to-talk waveforms, and also offers the option to dynamically partition the payload processing capabilities in response to cellular usage/demand patterns or other sensing/payload processing functions such as MIMO, adaptive equalization, beamforming, or STAP. Given the anticipated CONOPs of NSVs, a SWaP efficient multi-mission payload will likely be the preferred design option.

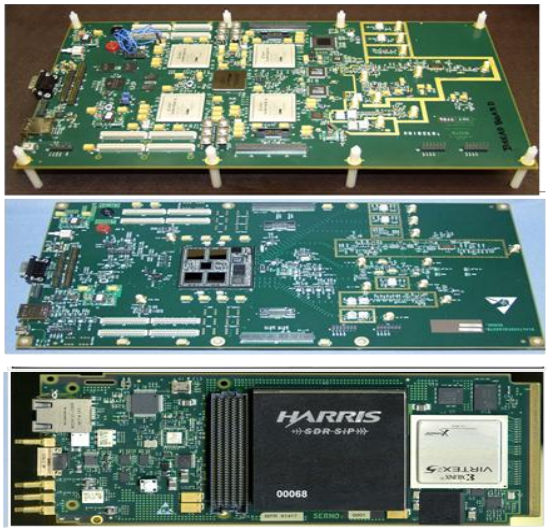

Figure 2-3: Evolution of the SiP-100 multi-mission platform from packaged parts development card (top), prototype SiP development card (center), and SiP deployment in an integrated µTCA implementation (bottom).

2.3 V4 Space Processor Radiation Hardness

For operation in a space environment the total ionizing dose (TID) and single event effects (SEE) require consideration. Additionally, the space environments are very different depending on the orbit (i.e. LEO, MEO, GEO, Molinya) and inclination. Shielding provides part of the solution, but shielding alone is often not practical. Hence, the V4 RSP is radiation hardened by design and part selection. The space processor, to meet the cost/performance objectives of the design, is specified to sustain a minimum total dose of 100 Krads before any performance degradation occurs, and 100Krad is feasible for most long duration LEO missions. However, for GEO mission life (e.g. 5 – 10 years), additional shielding is likely part of the solution.

The primary issue concerning this design is SEEs. SEEs can be extremely problematic for programmable devices, and are divided into three events classes

- Single Event Latchup (SEL)
- Single Event Upset (SEU)
- Single Event Transient (SET)

Our design philosophy has been to evaluate each part to ensure that they are immune from SEL (i.e. latch-up free), and to also characterize the SEU and SET events.

To mitigate the possible SEU and SET upset vulnerability the FPGAs V4 RSP uses two "on-board" methods:

- A "Watchdog ASIC" monitors each FPGA configuration memory during operation. The configuration is compared against the correct configuration (stored as a checksum in protected memory) and any detected errors are immediately corrected or "scrubbed". The scrubber power consumption depends on the scrubbing rate, which is user selectable to optimize power consumption for a given environment.
- The logic within the FPGA is augmented by selected Triple-Modular Redundant (TMR) storage and logic. A special development tool is used to triplicate the appropriate logic in the application. Voters are used to isolate an error and "vote" it out of the result providing corrected data on the fly.

These two techniques together deliver very high (>99%) availability, verified by radiation testing conducted at the Berkeley and Texas A&M accelerators while the V4 RSP performed as a high data rate MODEM.

The primary mechanism employed to mitigate SEE in the SDRAM is Error Detection and Correction (EDAC) coding. EDAC is used to protect the memory contents and it can correct any error that exists in any single nibble of a 32-bit word. A dedicated scrubber, housed in the "watchdog ASIC", reads every location in the SDRAM and validates the memory contents. The memory scrubbing rate is also programmable for possible power savings in various environments. Two spare SDRAM columns are provided in the memory array to allow the "watchdog ASIC" to "hotswap" these spare in for any other columns in the memory array as needed. We have used this memory architecture on several spacecraft.

Combined, these mechanisms reduce the cost of the system by allowing the use of commercial parts that meet Class S reliability and this memory architecture has been validated on several spacecrafts [6]. Any additional components have been screened to ensure that they meet the requirements for outgassing, total dose, and latchup.

III. V4 Space Processor in a Ka-band SDR

In support of the NASA Communications, Navigation, and Networking re-Configurable Testbed (CoNNeCT) program, Harris leveraged its existing SDP architecture to develop a high data rate Ka-band SDR. The CoNNeCT program is unique in that it will enable an SDR demonstration testbed on the International Space Station (ISS). Three different radios covering L-band, S-band, and Ka-band will be installed onboard the ISS and demonstrated as part of this program. The goal of this mission is to provide an operational testbed to demonstrate and exploit the features and benefits of SDRs on-orbit. Many different datarates, waveforms, frequencies, and coding techniques will be required, hence the need for reconfigurability in-situ and on-orbit.

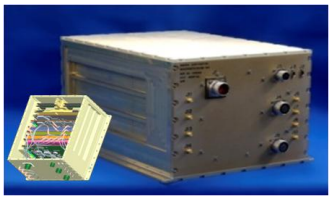

Figure 3-1: CoNNeCT Ka-band SDR Chassis.

The STRS compliant Ka-band radio delivered for this mission was based on the SDP architecture described above. Figure 3-1 shows the flight chassis designed around a 6U compact PCI open standard chassis which housed the majority of the payload elements. The Ka-band RF front end electronics is an external module to allow mounting at the antenna to optimize system performance. Figure 3-3 illustrates the overall payload architecture at the block level. A main feature of the design is the MODEM implemented with the Harris SDR based on the V4 processor. Again the common hardware architecture exploitable via software abstraction was a key enabler for the short design cycle and high performance.

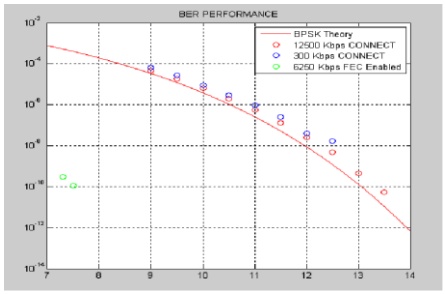

Figure 3-2: Sample CoNNeCT BER performance curve.

The Harris SDR has the ability to transmit up to 100 Mbps of user data rate coded with ½ rate error correction coding on the return link to the NASA tracking and data relay satellite system (TDRSS), and receive up to 25 Mbps on the uplink from TDRSS at Ka-band. Sample BER curves from lab tests are shown in the figure 3-2 versus theory. The FPGAs of the V4 processor were used to provide as much of the radio's functionality through the digital processor as possible. The radio digitally employed direct sampling of the intermediate frequency (IF) waveforms, a digital gain control algorithm, Doppler tracking filters, fine-tune frequency adjust, as well as the error coding, randomization, and other modem functions.

The CoNNeCT SDR is currently at a technology readiness level (TRL) of 8, system flight qualification through test and demonstration, and is scheduled to arrive at the ISS in 2012, where upon successful operation it will achieve a TRL of 9, system flight proven through successful mission operations. The the V4 RSP will be undergoing in-situ testing as part of the NASA CoNNeCT SDR on the International Space Station sometime in 2012 (planned).

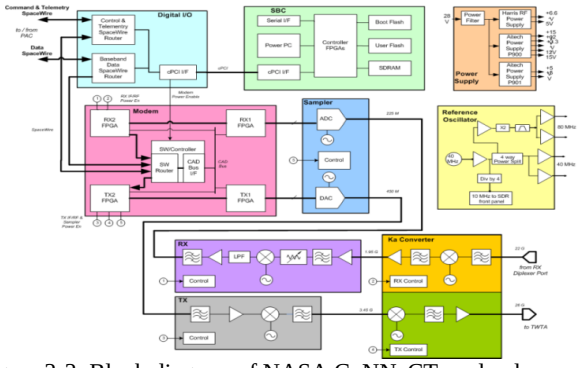

Figure 3-3: Block diagram of NASA CoNNeCT payload.

IV. The V4 Processor in Imaging RADARs

In order to demonstrate the simple re-purposing of the SDP architecture and core processing architecture reconfigurability to realize multi-mission capability, Harris embarked on a path to demonstrate an X-band radar capability in both lab demonstrations [9,12] and on-orbit demo of the AppSTAR™ concept. In both designs, Harris heavily leveraged the V4 processing architecture as a core processing component of a chirp RADAR payload. The re-purposing of the V4 platform into the lab RADAR waveform generator was completed, from inception to lab integration, in less than 10 weeks, owing again to the software tools and adherence to standards supporting straightforward re-configuring and managing of the on-board resources. For the spaceborne payload, the V4 processor framework has been initially loaded with waveform descriptors specific to that mission's objectives.

IV.1 V4-based Software Defined X-Band RADAR Lab Demo System

For the RADAR demo payload, the FPGA firmware was programmed to generate chirped linear frequency

modulated (LFM) transmit radar waveforms. This combined some external support RF X-band multiplier/frequency converter to provide a LFM waveform capability of up to 800 MHz of bandwidth (figure 4-1). Various parameters such as pulsewidth, chirp rate, start frequency, stop frequency, pulse repetition frequency (PRF), and number of pulses are easily modified given the software defined nature of the payload. The ability to dynamically alter the RADAR waveform so completely could provide a basis for cognitive RADAR capabilities, as well as supporting the dynamic mission needs for specific collection scenarios (e.g. resolution, EMI avoidance, spectral allocation, target/scene phenomenology). These features are currently under consideration in our research on remote sensing.

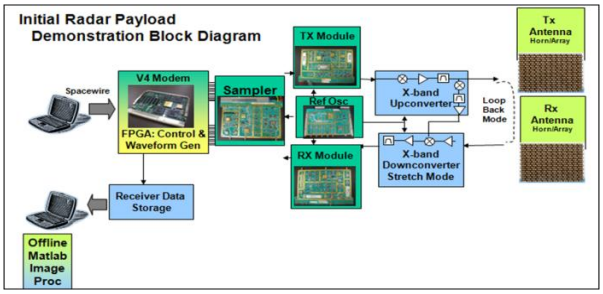

Figure 4-1: X-band software defined RADAR payload.

For initial lab demonstrations, a transmit pulse (400 MHz bandwidth) was digitally generated, frequency converted and multiplied up to X-band, and then looped back into the X-band receiver, pulse compressed by a swept stretch mode LO and digitized. The range Impulse Response (IPR) and Multiplicative Noise Ratio (MNR) were analyzed from the measured results [10]. The raw uncalibrated measured data shows nearly ideal main lobe shaping and acceptably low non-ideal sidelobe artifacts (figure 4-2). The only significant sidelobe energies of interest are the near-in lobes adjacent to the main lobe. These are due to deterministic phase errors and are easily removed through simple radar calibration techniques. However, even with these effects unmitigated the raw data exhibited an -23 dB MNR which meets typical allocations for RF radar electronics hardware.

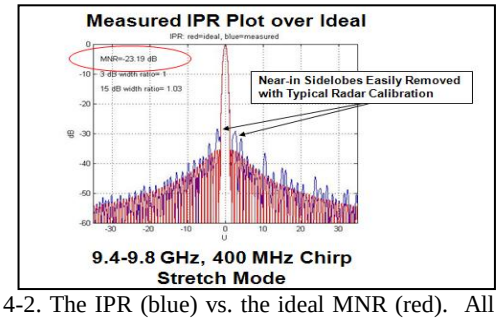

Figure 4-2. The IPR (blue) vs. the ideal MNR (red). All curves use Taylor weighted -35dB, nbar=5, per typical methodology.

To put the preceding result in a system context, the system and chirp waveform was tested as an inverse SAR (ISAR) RADAR. A simulated ISAR collect was performed on a ¼ scale model P-38 aircraft in an anechoic chamber (Figure 4-3). The RADAR waveform parameters were varied during the measurements with ultimate resolution capability of 0.25 m demonstrated which is typically 3x better than many commercial SAR systems. The ISAR images of the P38 scale model were formed by varying the RF chirp bandwidth using a constant chirp rate and varied pulse length. For the measurements shown, the frequency chirp slope rate was set to 40 MHz/usec and the pulse width was changed from 5 to 20 usec. At the highest resolution of 0.25m, the proportionate details of the plane's engines and fuselages, pilot cockpit, tail section, and wing-mounted fuel tanks were clearly recognizable.

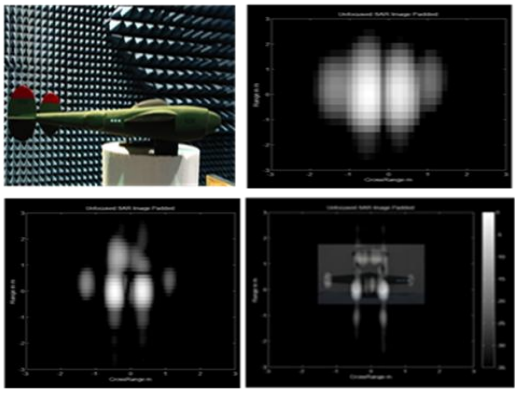

Figure 4-3: The lab mock-up of the P-38 and ISAR images at 1 m (top right), 0.5 m (bottom left), and 0.25 m (bottom right).

Plans are underway to build on the success of the lab demo system to dynamically switch payload from RADAR-only to a shared simultaneous RADAR/Comm system with waveforms dynamically loaded to meet real-time operational remote sensing and communication needs, again using the V4 re-configured in-situ.

IV.2 V4-BASED APPSTAR™ SPACE RADAR PAYLOAD

The V4 Space Processor card has been designated as the Reconfigurable Computing Element during the AppSTAR™ development to better reflect its multi-function usage and in response to a few enhancements incorporated to better match its true multi-mission role in AppSTAR™ concept. For the initial application configuration, as has been discussed on the RADAR lab demonstrations, an entire Synthetic Aperture RADAR (SAR) data collection application has been developed. This encompasses transmit waveform generation, including digital pre-correction of the wideband pulses (> 500 MHz) for IF/RF line-up imperfections such as gain slope, ripple and phase deviations from ideal linearity, and precise timing control of transmit and receive processing functions for both stripmap and spotlight modes as well as for the stretch (de-chirped) and matched filter operations [10]. Simultaneous receive processing, all hosted on the V4 fabric, includes digital quadrature down-conversion, mission selectable filtering and adaptive re-quantization of

returns to accommodate limited downlink resources while maintaining image quality.

Digital output compensation follows the Harris joint RF and digital system design philosophy of meeting operating requirements in a joint system-oriented fashion. This allows the RCE, coupled with the RF up-conversion electronics, to meet the expected mission MNR and IPR error budget allocations while minimizing overall system design and development cost.

The entire application load for the SAR mission easily fits within the four V4 FPGA fabric with significant margin and includes the extensive IO Wrapper designs used to abstract all hardware level IO interfaces. These consist of: A/D and D/A interfaces, CAD Bus, SERDES, Fiber Channel, chip-to-chip parallel IO, clock and enable high-speed transport and multiplexed Test Ports on each FPGA. The VHDL implementation follows a model-based design flow starting from a bit-exact behavioral model developed in MATLAB/Simulink to provide bit-true test vectors for all processing functions and data conversion interfaces. The model-based design approach along with the extensive use IO abstraction minimizes development and intergration time for an application by as much as 30%.

One of the enhancements to the RCE was to expand the on-board storage capacity to support four full application images for all four FPGAs. This allows the AppSTAR^{TM} platform to support four concurrent missions with the ability to execute any two within a single orbit. Re-configuration and initialization can be accomplished in < 5 seconds once an uplink re-configuration command is received.

5. CONCLUSIONS

The adaptability and configurability of this space-qualified AppSTAR^{TM} SDP architecture quickly enables the payload development of communications, radar and other missions. The AppSTAR^{TM} concept, with the V4 and SiP-100 as processing cores, has proven valuable by supporting new and changing mission objectives, additional waveforms, and signal processing algorithms. Going forward SDPs can be assembled from processing elements and dynamically programmed in –situ to adapt to rapidly changing mission profiles, thereby extending mission life and increasing the value of platforms. Additionally the commonality of the processing core reduces mission life-cycle cost by decreasing the NRE incurred in new system designs.

Operational experience has shown that the V4 processor can be completely reprogrammed through industry standard interfaces and begin operating in a new configuration in < 15 seconds. This level of adaptability yields unprecedented dynamic mission flexibility for a multi-mission capable payload. It also opens the possibility to consider on-board autonomous controllers to manage the sensor timelines to address prioritized mission elements when configured in a multi-mission payload.

Work is planned to continue evolving AppSTAR^{TM} payload concepts with the SiP-100 and V4 Space Processor to incorporate more complex capabilities to address the emerging areas of cognitive radios and dynamic spectrum access in conjunction with advanced remote sensing capabilities, signal analysis/recognizers, and other specialized needs.

6. REFERENCES

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