Simple QPSK Modulator Implemented in Virtex 6 FPGA Board for Satellite Ground Station

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Abstract - *Modulation is a key feature commonly used in wireless communication for data transmission and to minimize antenna design. QPSK (Quadrature Phase Shift Keying) is one type of digital modulation technique used to transfer the baseband data wirelessly in much efficient way compare to other modulation techniques. Conventional QPSK modulator operates by separation of baseband data into i and q phases and then add them to produce QPSK signal. The process of generating sine and cosine carrier wave to produce the i and q phases consume high power. For better efficiency in power consumption and area utilization, 2 new types of QPSK modulator proposed. The proposed method will eliminate the generation of 2 phases and will produce the QPSK output based on stored data in RAM. Verilog HDL used to implement the proposed QPSK modulators and it has been successfully simulated on Xilinx ISE 12.4 software platform. a comparision has been made with existing modulator and significant improvement can be seen in term of area and power consumption.*

Keywords: QPSK, Verilog, Modulation

1 Introduction

Continuous growing demands from end user for more data have encouraged the engineers to develop many new types of modulation scheme in satellite communication system. New types of modulation technique introduced to increase the efficiency in data transmitting and receiving rate within the same bandwidth. One of the common modulation method used in satellite communication system is QPSK which is one form of PSK (Phase Shift Keying) modulation scheme [7]. In PSK modulation, the phase changed according to the baseband data while the frequency and amplitude remain unchanged. In QPSK quadrature means 4 different states that is used to represent a group of 2 bits input data. The four different inputs are 00, 01, 10 and 11 and each group takes one form of QPSK states as shown in table 1.

Table 1: QPSK phase with different input.

Input	QPSK phase
00	135˚
01	225˚
10	45˚
11	315˚

The other most related to QPSK modulation scheme is BPSK (Binary Phase Sift Keying) modulation. In more practical understanding, QPSK is formed from 2 separate BPSK which combined together. However, the data transmission in QPSK is twice when compared to BPSK and the Bit Error Rate (BER) over signal to noise ratio (SNR) for both modulation schemes are same [8]. The symbol period for QPSK is 2 times the bit period, $Ts=2Tb$ while for BPSK the symbol period is same as bit beriod $Ts=Tb$ [1,9]. Data transmission rate is very crucial for Low Earth Orbital (LEO) satellite system where the interaction time with earth ground station is very short. Implementing QPSK in full digital domain not only can save cost for long term but at the same time, it increases the wireless data immunity over surrounding noise [8]. The high configurability and MIPS (million instructions per second) in FPGA (Field Programmable Gate Array) have made the implementation of digital signal processing possible.

2 Conventional modulator

The conventional QPSK modulator operates by dividing the baseband data into 2 main streams, even and odd data. The divided unipolar data then changed into bipolar by using NRZ encoding technique. Continuously, the coded data will be mixed with carrier, which generated from DDFS (Direct Digital Frequency Synthesizer) or also known as DDS (Direct Digital Synthesizer) as shown in figure 1. The DDFS produced the sine and cosine as separate carrier wave signal and it made the mixing process much easier. The intended frequency use for transmission can be set while generating the DDFS core in Xilinx Integrated Software Environment (ISE) [11]. Xilinx provides the DDFS as IP CORE in ISE 11.3 and above version. The DDFS version 4 can produce up to 550

MHz carrier wave. After the process of carrier mixing, the odd data will known as I phase and the even data as Q phase.

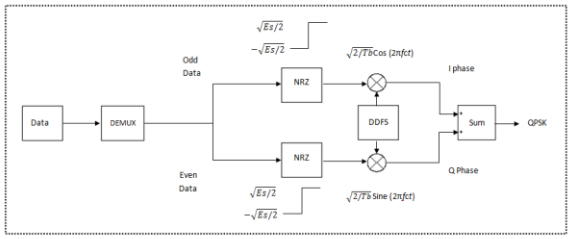


Figure 1: Conventional QPSK modulator block diagram

Table 2 shows the even and odd data represented by I and q phases. These two phases will be added to produce the QPSK signal. The general QPSK wave can be expressed as shown in equation (1) where i equal to 1, 2, 3 or 4, Es represent energy for a symbol,Ts represent period for a symbol and fc represent the carrier frequency.

$$QPSK = \sqrt{\frac{2Es}{Ts}} cos(2\pi fct + \frac{(2i-1)\pi}{4}) \qquad (1)$$

Table 2: NRZ coded odd and even data converted into I and q phase

odd Data	Even data	I phase	Q phase
-1	-1	$-\cos \omega_c t$	$-\sin \omega_c t$
-1	1	$-\cos \omega_c t$	$\sin \omega_c t$
1	-1	$\cos \omega_c t$	$-\sin \omega_c t$
1	1	$\cos \omega_c t$	$\sin \omega_c t$

3 Proposed QPSK modulator

The conventional method used to generate the QPSK signal consumes high power and area in FPGA. The proposed QPSK modulators are fully digital domain and produced QPSK output same as equation (1). The 2 new proposed QPSK modulators used RAM as main data storage to produce same QPSK signal as conventional modulator.

3.1 Proposed QPSK modulator 1

The first proposed QPSK modulator is designed in 2 steps. In first step, the above conventional architecture will be constructed just to collect different QPSK phase data for combinational input data. Once intended data collected, the conventional architecture will not be used for future QPSK signal generation. This will be major dynamic power saving since the DDFS will not be used to generate the 2 different carriers. Collected QPSK data will be stored in 4 different RAMs. Each RAM will store data for one QPSK phase. The multiplexer will be used to choose the correct RAM's according to the splitted input data. Table 3 shows the associated RAM's with different inputs and phases. Figure 2 shows the block diagram for the first proposed QPSK modulator.

Table 3: QPSK phase data stored in 4 Different RAMs according to input data.

RAM	QPSK Phase	Input Data
RAM # 1	135°	00
RAM # 2	225°	01
RAM # 3	45°	10
RAM # 4	315°	11

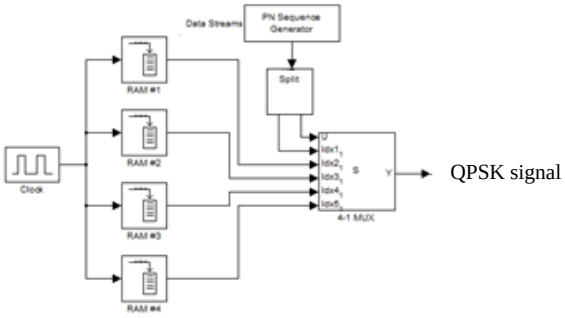


Figure 2: Block diagram for proposed QPSK modulator 1.

3.2 Proposed QPSK modulator 2

As for the second QPSK modulator architecture proposed, further reduction have made from the first architecture. Only 1 block RAM used instead of 4 RAM as in first design. The general equation for QPSK as in (1), give us information that the whole QPSK wave can be represented by a single phase shifted cosine wave. A single cosine wave with different phase representing one symbols in QPSK modulation. With that info, data to generate a cosine wave stored in RAM and for different input data, a pointer assigned at specific RAM address to retrieve the exact phase that needed to generate QPSK wave. Figure 3 show the second proposed QPSK modulator block diagram.

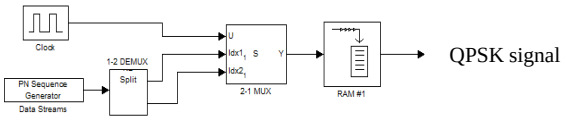


Figure 3: Block diagram for proposed QPSK modulator 2.

4 Simulation

Both proposed designs and conventional QPSK modulator modeled with Verilog HDL and simulated on Xilinx ISE platform. The crucial for simulate the conventional QPSK modulator is for comparison with the other two proposed architecture in term of power and area utilization in FPGA. Each of the design Verilog HDL code synthesizes and tested with a test bench code to simulate it functionality. The synthesizable code translated into RTL(Register Transfer level) schematic diagrams while the Xilinx ISim simulator used to run the test bench code to obtain timing diagram. The simulator also used to produce the decimal data which later used in Microsoft office Excel to plot the waveforms.

4.1 Conventional QPSK modulator

Figure 4 shows the RTL obtain from systhesize Verilog HDL code for conventional QSPK modulator while figure 5 shows a portion of timing diagram where the data (even and odd) change from 00 to 01. The QPSK wave is represented as sum (concatination of Cout and S) of I and Q phase in the timing diagram . Decimal data collected for QPSK wave, I and Q phases from the timing simulation used to plot the waveform .

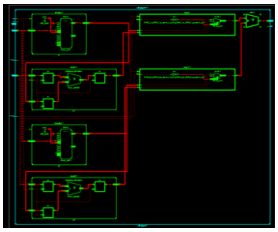
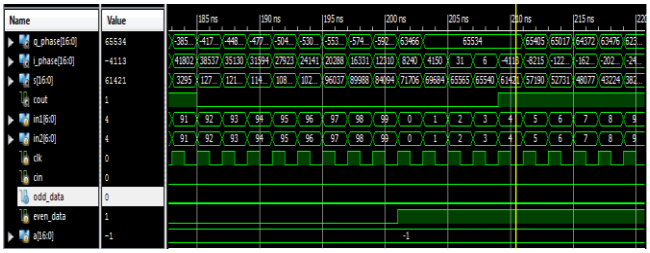


Figure 4: Top level RTL for conventional QPSK modulator



Figre 5: Timing analysis demonstrates a portion of even and odd data transition.

4.2 Proposed QPSK modulator 1

Figure 6 shows the RTL schematic diagram and figure 8 shows timing diagram for proposed QPSK modulator 1. Since the architecture no longer separate the baseband data into 2 single bit (even and odd baseband data), a group of 2 bits used to represent a phase in QPSK waveform. A total number of 100 data stored in each RAM to represent a phase in QPSK wave. Each data need 2 ns (one clock period) and for 100 data 200 ns needed to form a phase. Figure 7 shows the baseband data transition from 01 to 10.

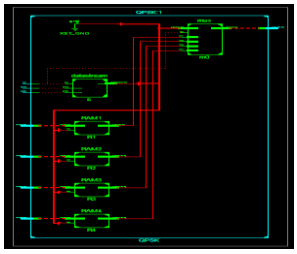


Figure 6: RTL diagram for proposed QPSK modulator 1

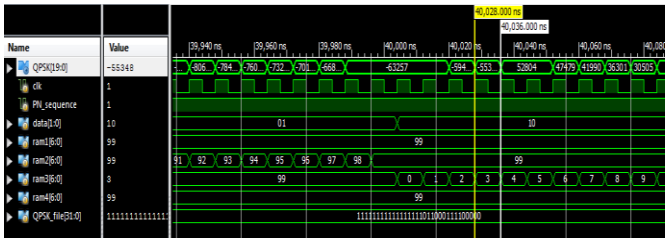


Figure 7: Timing diagram for proposed QPSK modulator 1

4.3 Proposed QPSK modulator 2

As for the proposed QPSK modulator 2, figure 8 shows the RTL schematic diagram and figure 9 shows the timing diagram. 100 data stored in one RAM to represent a complete cosine waveform and a counter assigned to access the data for a specific phase. The timing diagram shows the transition of baseband data from 11 to 00.

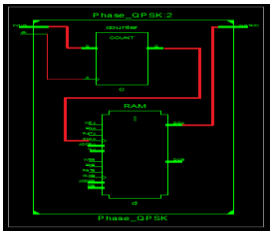


Figure 8: RTL schematic diagram for proposed QPSK modulator 2.

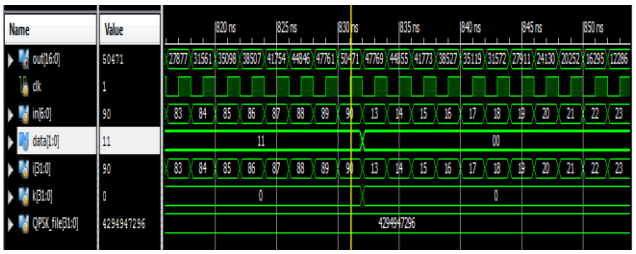


Figure 9: Timing diagram for proposed QPSK modulator 2.

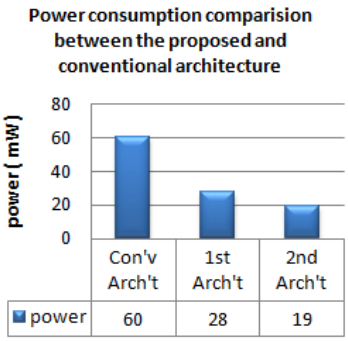


Chart 1: Power consumption for different architecture.

5 Discussion

Power consumption and area utilization is 2 main criteria studied in this project. Both criteria play major roles when the FPGA design translated into ASIC.

5.1 Power

Xilinx provide 3 types of power analysis tools where different tools perform power analysis at different stages. The Xpower estimator tool usually used in the predesign and preimplementation phases of a project [4]. While the XPower Analyzer (XPA) tool performs power estimation at post implementation stages [10]. It is the most accurate tool since it can read from the implemented design database the exact logic and routing resources used for a design. The last power analyzer tools provided by xilinx is PlanAhead RTL power estimator. This software provided an earlier stages of power and area utilaization of a desgin at RTL level. PlanAhead reads the HDL code from a design to estimate the resources needed, and reports the estimated power from a statistical analysis of the activity of each resource [5]. Since the PlanAhead provide an ealier power consumption and area utilaization analysis at same time,the software used instead of the other two power tools analyzer. Chart 1 shows the power comparison between the poposed and conventioanal QPSK modulator. Its cleary shows that the power consumption for both proposed QPSK modulator consume much more less power compare to the typical QPSK modulator architecture using the DDFS. The 1st architecture consume 32mW and the 2nd arcthitecure consume 41mW less power than the conventional architecture. The power analysis mainly carried out on device static power or leakage power where the transistor in FPGA use to hold the device configuration. However it is also known that the FPGA consumed more power compare to ASIC. The power consumption is high in FPGA due to it flexibity in configuration and rerouting . So when the proposed design implemented in ASIC where only dedicated number of transistor used for that design,more power consumption can be reduced.

5.2 Area

Area employment by number of gates in FPGA can directly influence the power consumption, reliability and the cost of a design. A simple design can cut or reduce the number of gates occupied in FPGA and at the same time increase the performance indirectly. The proposed 2nd architecture dramatically consumed more less gates compare to the conventional and the 1st proposed architecture. Even though the 1st architecture have almost double number of LUT from the conventional QPSK modulator, but the power consumption is still less when compared. This is mainly because the 1st architecture proposed does not employ DDFS, DSP48 and arithmetic logic blocks as in the conventional design. Chart 2 shows the number of LUT and I/O used for the proposed and conventional architecture.

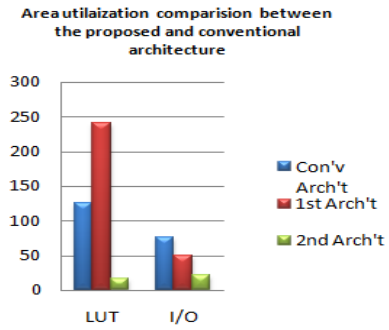


Chart 2: Area utilization in FPGA for different architecture.

6 Conclusion

The proposed QPSK modulators successfully simulated on Xilinx ISE 12.4 software platform and the results obtain shows that the output waveform is same as conventional QPSK modulator. The power analysis tools used on analyze the power consumption and area utilization on the proposed modulator also gives positive feedback. Both proposed architecture consume less power when compared with

conventional architecture. As for future plan, both designs will be implemented on virtex 6 FPGA board and RF front end module will be used to transmit the baseband data. A functional demodulator also will be constructed to retrieve the wirelessly transmitted baseband data.

7 References

[1] M.Kovac, J.kolouch "BPSK, QPSK Modulator Simulation Model" 2004.

[2] Teena Sakla, Divya Jain, Sandhya Gautam "Implementation of Digital QPSK Modulator by Using VHDL /MATLAB" International Journal of Engineering and Technology Vol. 2(9), 2010.

[3] Gihad Elamary,graeme Chester,Jeffrey Neasham " A Simple Digital VHDL QPSK Modulator Designed Using CPLD/FPGAs for Biomedical Devices Application" Proceeding of the World Congress on Engineering Vol 1,2009.

[4] User Guide for Xilinx XPower Estimator, www.xilinx.com/support/documentation/user_guides/ug440.pdf

[5] User Guide for Xilinx Plan Ahead, http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/PlanAhead_UserGuide.pdf

[6] Jouko Vankka, "Direct Digital Synthesizers: Theory, Design and Application", 2000.

[7] Explaination about QPSK modulation, www.complextoreal.com

[8] Bit Error Rate over Signal to Noise Ratio, http://en.wikipedia.org/wiki/File:PSK_BER_curves.svg

[9] Václav VALENTA, "Error Performance of BPSK and QPSK in Satellite Communications".

[10] LogiCORE IP DDS Compiler v4.0 http://www.xilinx.com/support/documentation/ip_documentation/dds_ds558.pdf

[11] User Guide for Xilinx Xpower Analyzer, http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/ug733.pdf